The First IEEE International Workshop on LLM-Aided Design (LAD'24)

June 28-29, 2024
IBM Research
Almaden, San Jose, CA

Day 1: June 28th

8:15am-8:45am Breakfast

8:45am-9:10am Opening remarks

9:10am-10:10am Keynote 1: Reasoning Myths about Language Models: What is Next?

Speaker: Dan Roth, VP/Distinguished Scientist, AWS AI Labs & Eduardo D. Glandt Distinguished Professor, UPenn. Abstract and Bio

Session Chair: Deming Chen

10:10am-10:30am Coffee Break

10:30am-Noon **Best Paper Nominees,** 15 min talks (12 min + 3 for Q&A)

Session Chair: Jose Renau, UCSC

AMSNet: Netlist Dataset for AMS Circuits (Zhuofu Tao, Yichen Shi, Yiru Huo, Rui Ye, Zonghang Li, Li Huang, Chen Wu, Na Bai, Zhiping Yu, Ting-Jung Lin, Lei He)

VerilogReader: LLM-Aided Hardware Test Generation (Ruiyang Ma, Yuxin Yang, Ziqian Liu, Jiaxi Zhang, Min Li, Junhua Huang, Guojie Luo)

RTLCoder: Outperforming GPT-3.5 in Design RTL Generation with Our Open-Source Dataset and Lightweight Solution (Shang Liu, Wenji Fang, Yao Lu, Qijun Zhang, Hongce Zhang, Zhiyao Xie)

EDA Corpus: A Large Language Model Dataset for Enhanced Interaction with OpenROAD (Bing-Yue Wu, Utsav Sharma, Sai Rahul Dhanvi Kankipati, Ajay Yadav, Bintu Kappil George, Sai Ritish Guntupalli, Austin Rovinski, Vidya Chhabria)

MG-Verilog: Multi-grained Dataset Towards Enhanced LLM-assisted Verilog Generation (Yongan Zhang, Zhongzhi Yu, Yonggan Fu, Cheng Wan, Yingyan Celine Lin)

Large Language Model (LLM) for Standard Cell Layout Design Optimization (Chia-Tung Ho, Haoxing Ren)