# A Collaborative Machine Learning Approach to Fast and High-Fidelity Design Prediction

*Task 2810.021*
*Jiang Hu*
*Dept of ECE*
*Texas A&M University*

*Task 2810.022*
*Yiran Chen*
*Dept of ECE*
*Duke University*

# Task Overview

- Center: Texas Analog Center of Excellence (TxACE)
- Thrust: Computer-Aided Design and Test (CADT)
- Subthrust: System, Logic and Physical Design (SLPD)
- Task leaders
  - Jiang Hu, Texas A&M Univ, Task 2810.021
  - Yiran Chen, Duke Univ, Task 2810.022
- Start date: January 1, 2019
- Industrial liaisons
  - Gi-Joon Nam, IBM
  - Xiaoqing Xu, ARM
  - Divya Prasad, ARM
  - Savithri Sundareswaran, NXP

# Anticipated Results

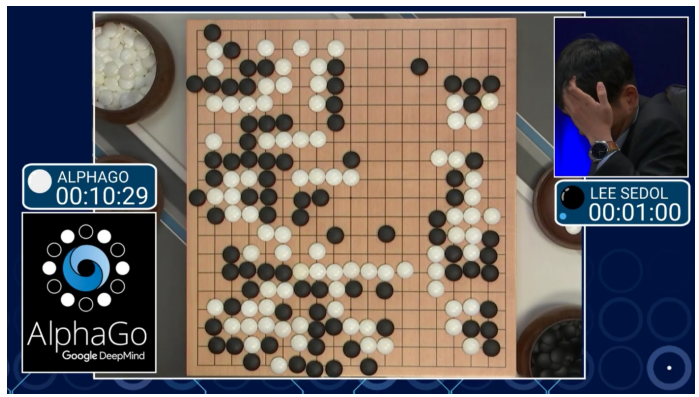
- Machine learning-based techniques for fast and high-fidelity prediction of
  - circuit routability
  - timing
  - power
  - crosstalk noise
- Routability/crosstalk predictions will be useful for analog and mixed-signal designs
- Will show how the predictions improve macro/cell placement and system level models

# Planned Deliverables

- Machine learning-based early routability prediction for digital and analog IC designs. (12/2019)
- Machine learning-based early timing prediction for digital IC designs. (12/2019)
- Machine learning-based early crosstalk noise prediction for digital and analog IC designs. (12/2020)
- Machine learning-based early power prediction for digital IC designs. (12/2020)
- Machine learning-guided placement for routability, timing, power and signal integrity improvement. (12/2021)
- Application of machine learning-based prediction in system-level models for hardware IPs. (12/2021)

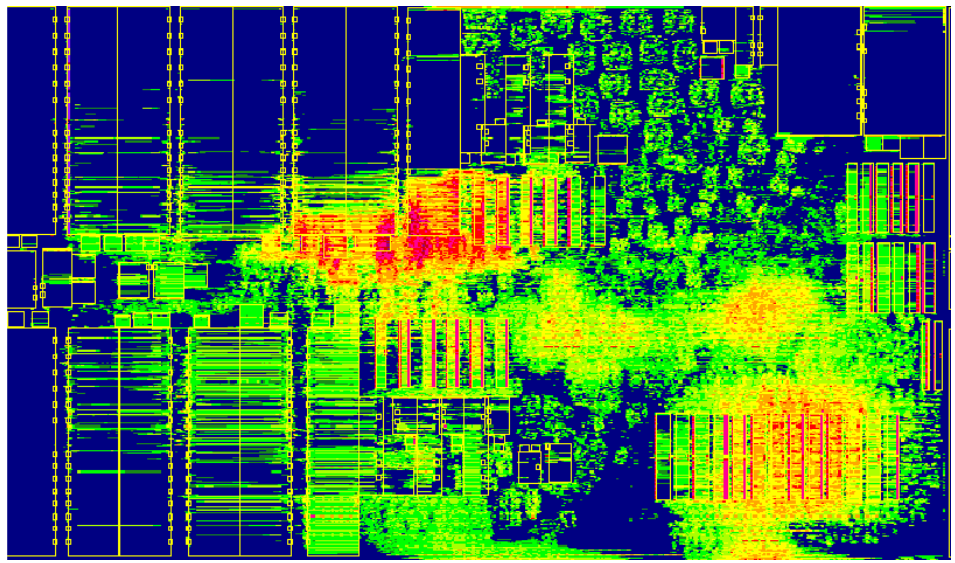
# Background and Motivation

- Decisions in early design steps have large impact
- Need fast and high-fidelity predictions
- Existing techniques
  - Analytical: fast but inaccurate
  - Trial design: accurate but very slow
- Machine learning
  - Extracting design knowledge from data
  - Emulating design experience



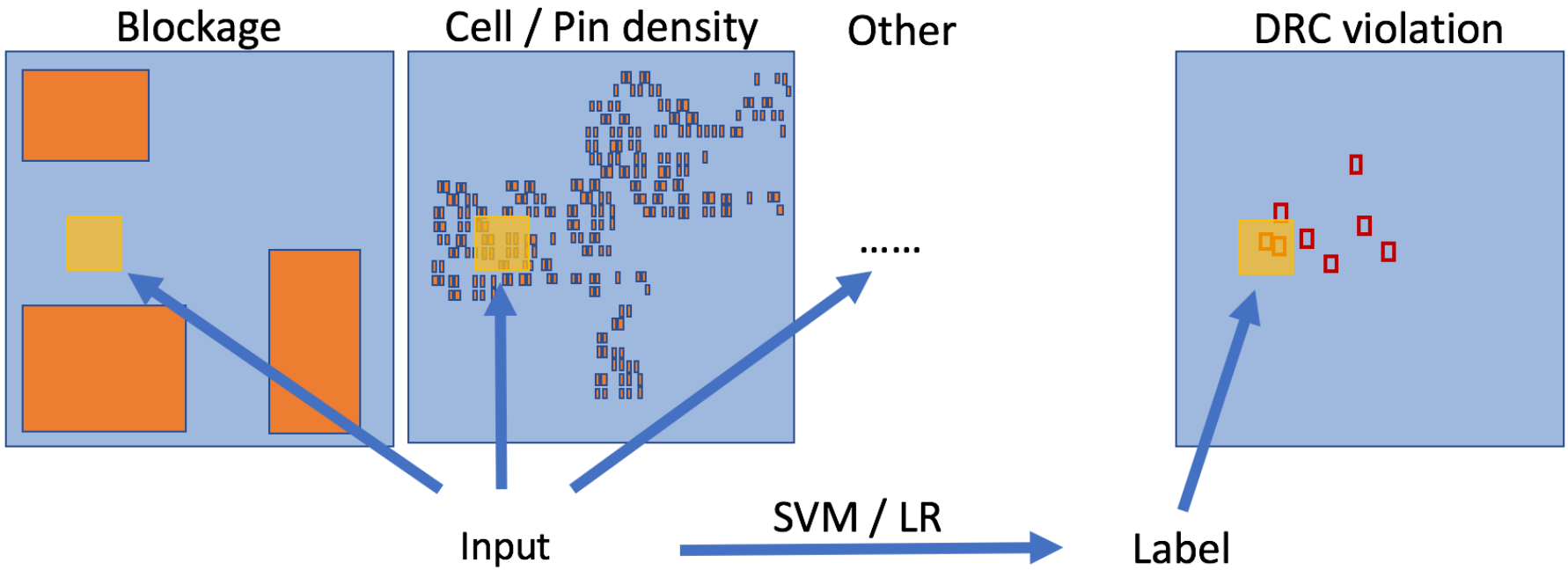
# Early Routability Prediction

- Routability: post-routing design rule violations
- Early prediction at placement stage
- Analytical techniques
  - Very fast
  - Not enough fidelity
- Trial routing
  - Acceptable fidelity
  - Not fast enough



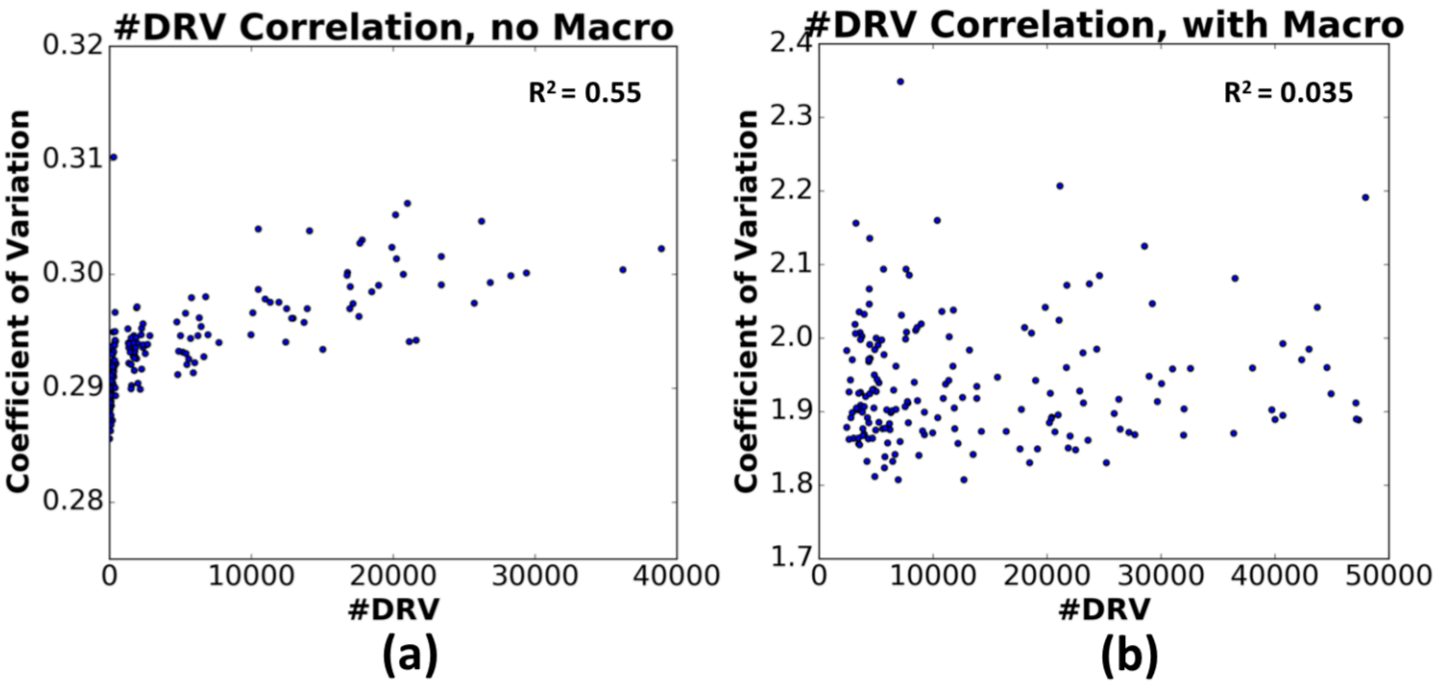
# Prior Machine Learning Approaches

Learning on ***small*** *cropped regions*



# Placement with Macros

- Layout is less homogeneous
- Correlation between pin density and #DRV becomes weak



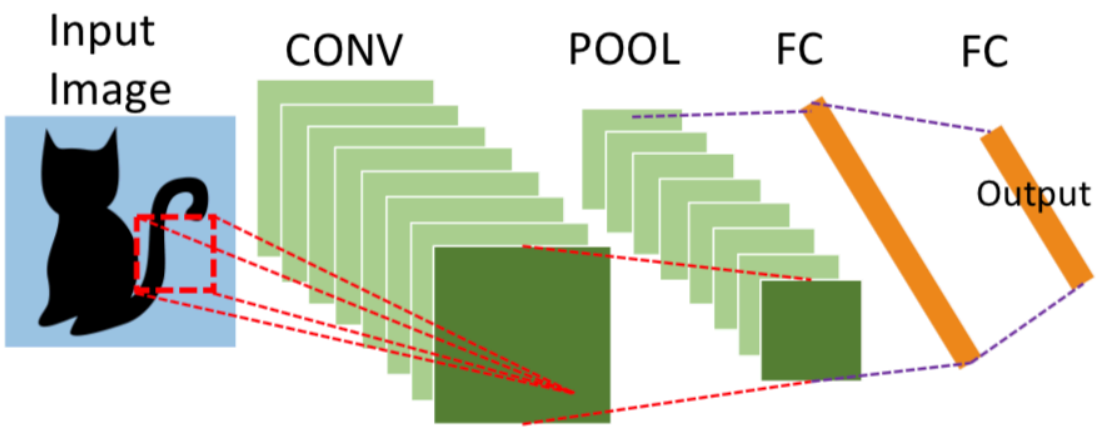

Each point corresponds to one placement

# Problem Formulations

- Predicting overall number of design rule violations (#DRV)
  - Given two placement solutions, tell which is more routable with high fidelity
- DRV hotspot detection
  - Given a relatively routable placement solution, pinpoint DRV hotspots such that mitigation measures are well targeted

# CNN for #DRV Prediction

Given a cell placement, classify it among four routability levels, $c_0$, $c_1$, $c_2$, $c_3$, $c_0$ has the least #DRVs

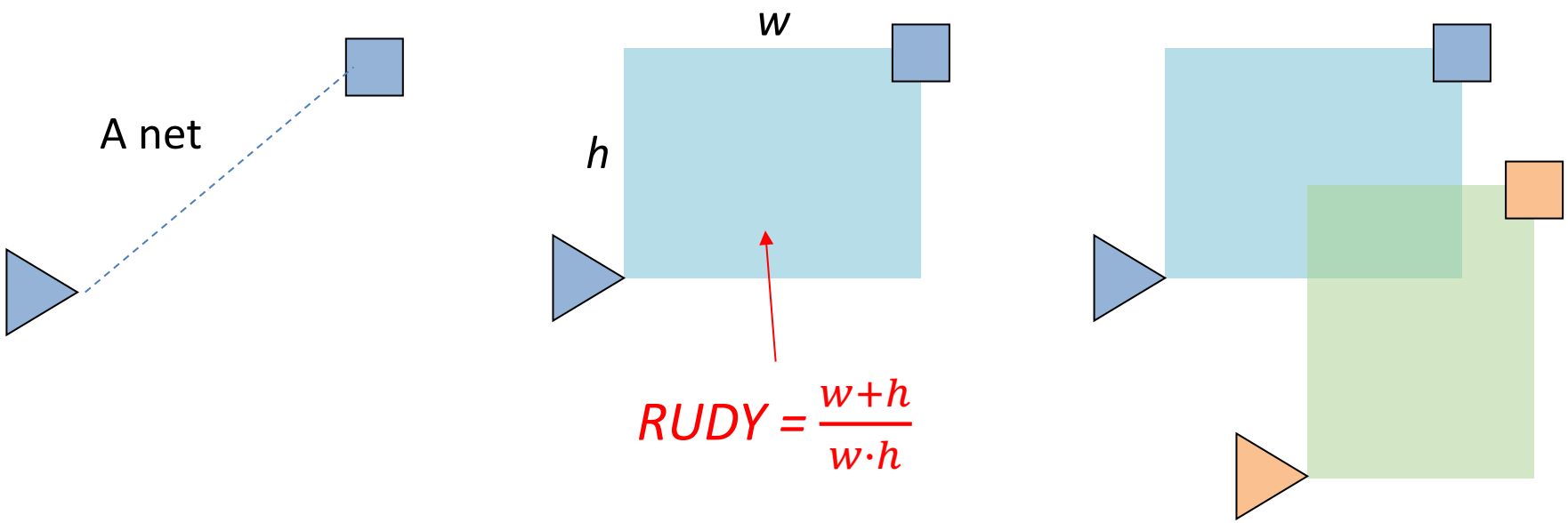



Convolutional (CONV), Pooling (POOL) and Fully Connected (FC) layers

Widely used in image classification

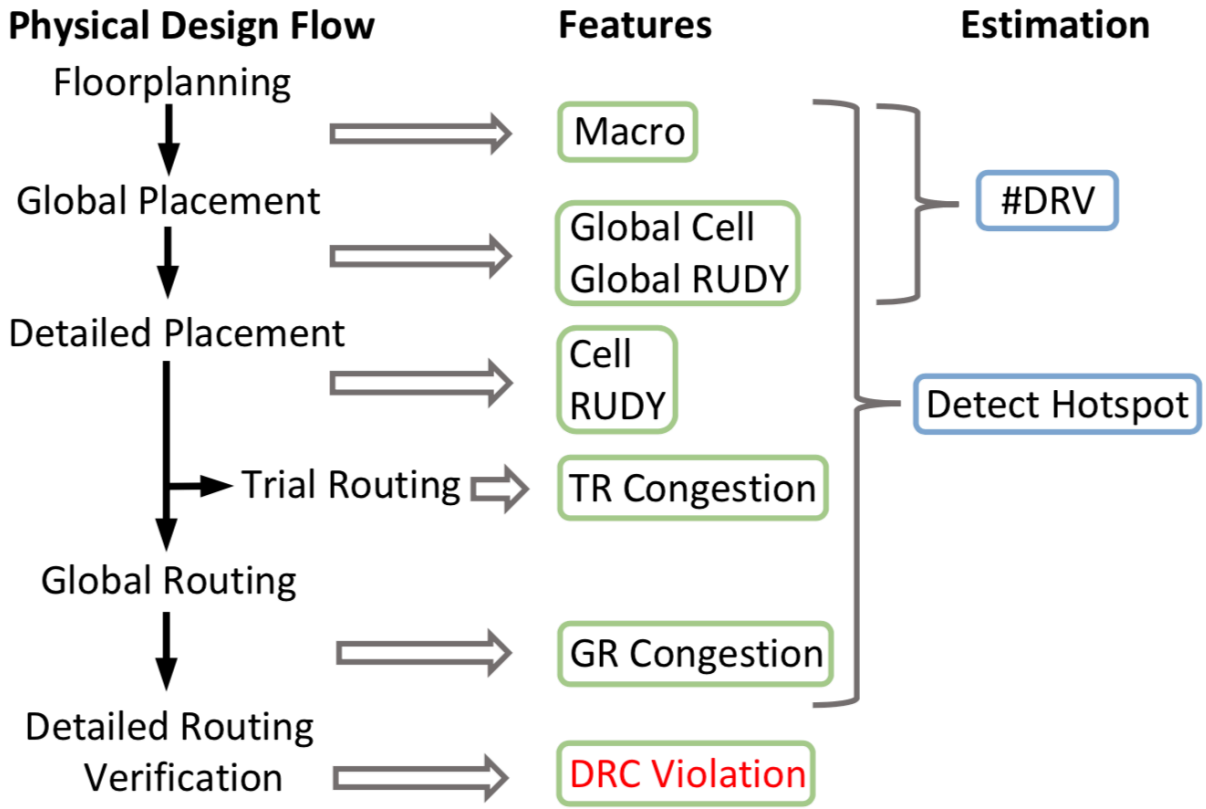
# An Important Feature

- RUDY (Rectangular Uniform wire DensitY) (P. Spinder et al. DATE07)
- RUDY at a point is superposition of RUDYs of multiple nets



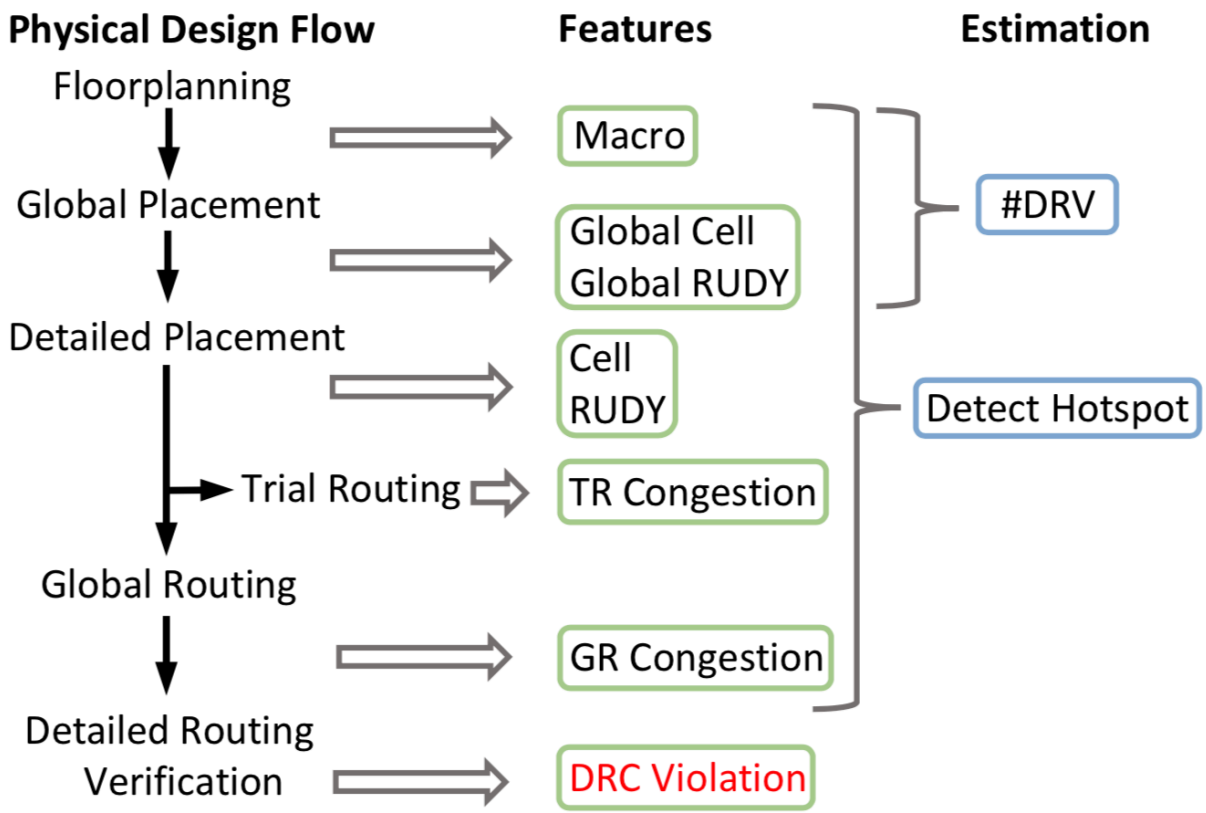
# Features for #DRV Prediction

- Macro:
  - region occupied by macros
  - density of macro pins in each layer
- Cell:
  - density of cells
  - density of cell pins
- Global cell:
  - cell features at global placement
- Global RUDY:
  - RUDY features calculated by global placement results

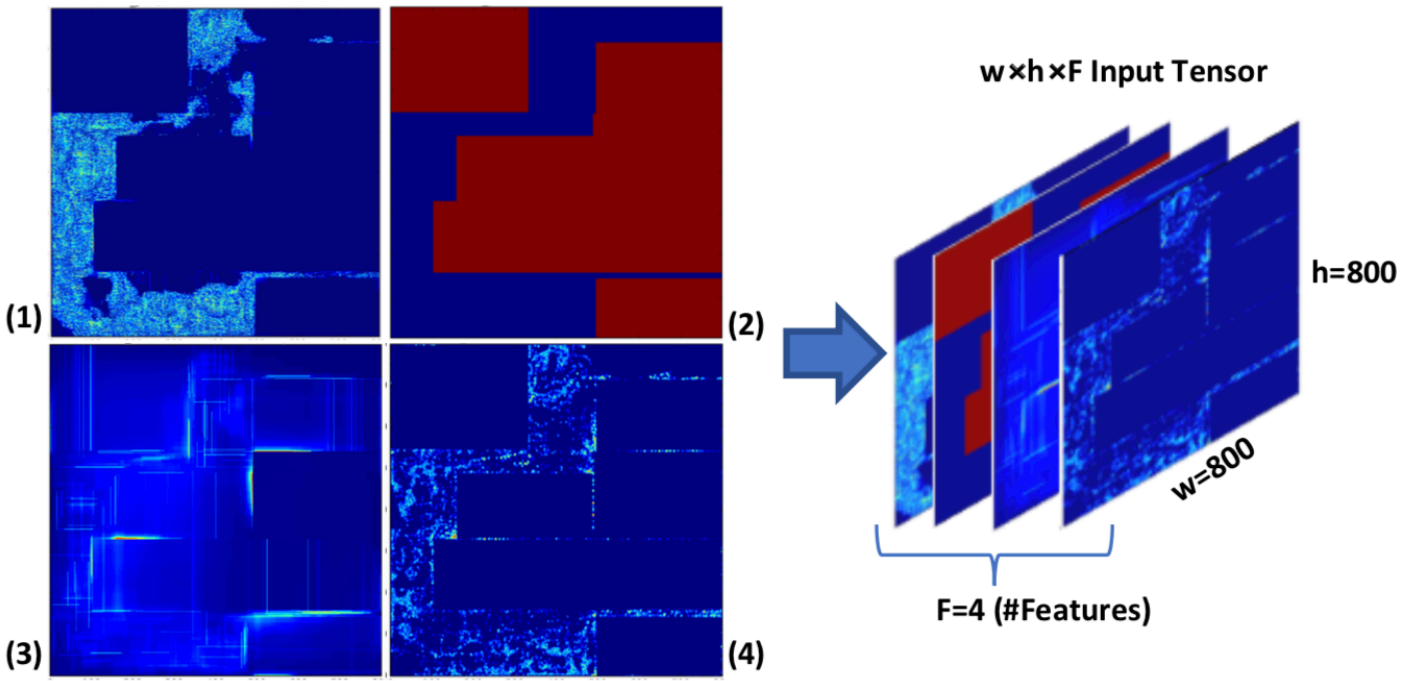


# Other Features

- RUDY
  - long-range RUDY
    - RUDY from long-range nets
  - short-range RUDY
    - DURY from short-range nets
  - RUDY pins
    - pins with density value equal to the RUDY value of its net
- Congestion
  - trial global routing congestion
  - global routing congestion
- DRC violation
  - prediction target / label

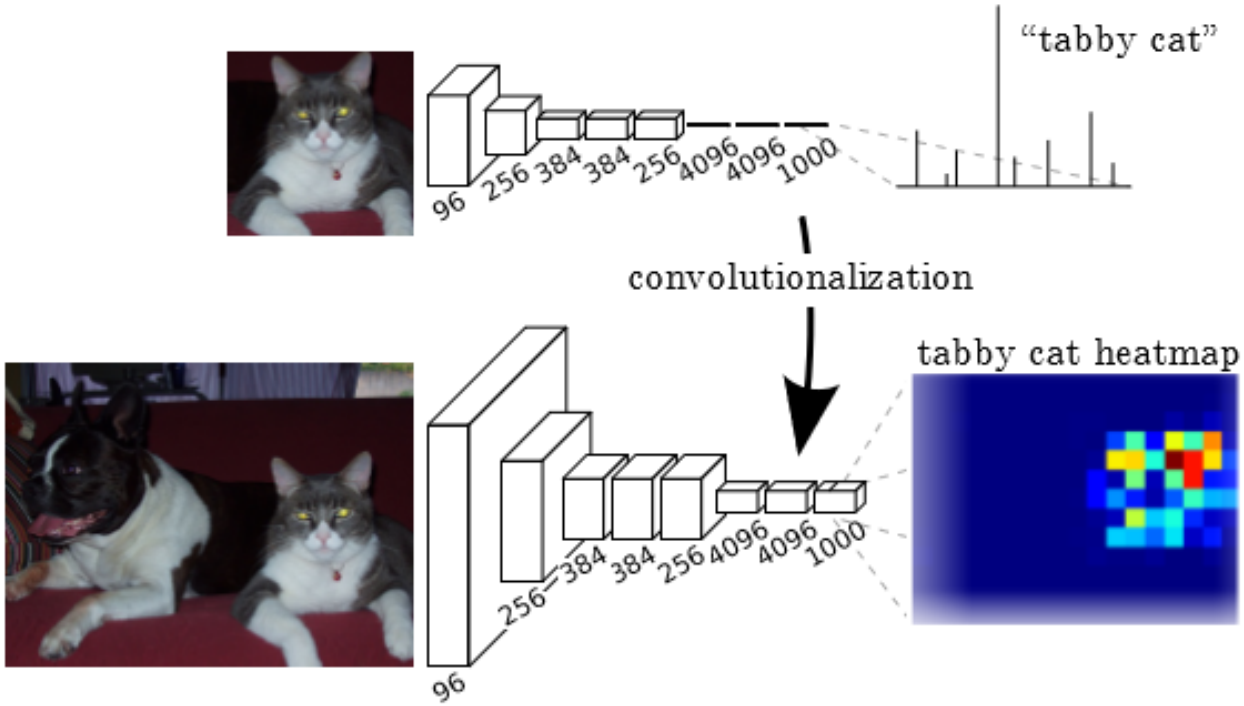


# Feature Illustration




Input tensor constructed by stacking 2D features:
(1) Pin density, (2) macro (3) long-range RUDY, (4) RUDY pins

# Fully Convolutional Network for Hotspot Prediction




Eliminate FC layers

May use transposed-convolutional to up-sample

Used in image segmentation, object detection

# Experiment Setup

- Five designs from ISPD 2015 placement contest, 45nm technology
- ~300 different placements by placing macros in different ways
- Placement, routing and DRC are done by Cadence tool
- When a circuit is tested, the model trained with the other circuits
- SVM and Logistic Regression (LR) methods for comparison

| Circuit Name | #Macros | #Cells | #Nets | Width (μm) | #Placements |
|---|---|---|---|---|---|
| des_perf | 4 | 108288 | 110283 | 900 | 600 |
| edit_dist | 6 | 127413 | 131134 | 800 | 300 |
| fft | 6 | 30625 | 32088 | 800 | 300 |
| matrix_mult_a | 5 | 149650 | 154284 | 1500 | 300 |
| matrix_mult_b | 7 | 146435 | 151614 | 1500 | 300 |

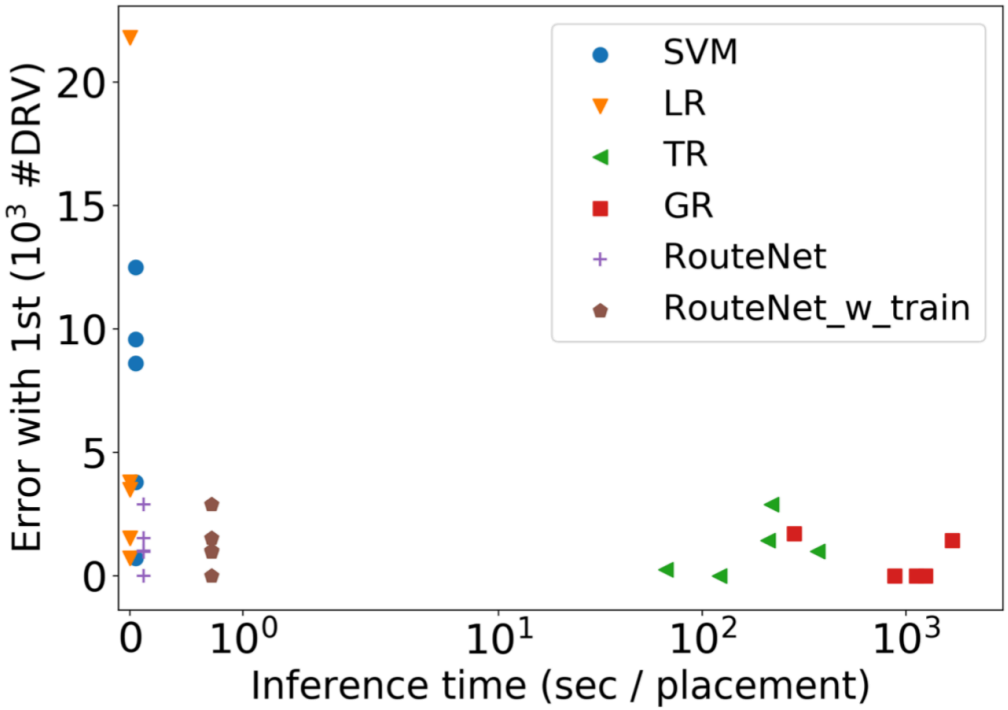
# #DRV Prediction Fidelity

- How recognize placements with the lowest #DRV level ($c_0$)
- The **best rank** of top ten placements predicted to have least #DRV

| Circuit Name | $c_0/c_1+c_2+c_3$ accuracy (%) | | | | | Best rank in top 10 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | SVM | LR | TR | GR | Route Net | SVM | LR | TR | GR | Route Net |
| des_perf | 63 | 74 | 80 | 77 | 80 | $87^{th}$ | $15^{th}$ | $2^{nd}$ | $1^{st}$ | $2^{nd}$ |
| edit_dist | 69 | 68 | 78 | 77 | 76 | $17^{th}$ | $17^{th}$ | $3^{rd}$ | $3^{rd}$ | $2^{nd}$ |
| fft | 66 | 62 | 73 | 70 | 75 | $6^{th}$ | $6^{th}$ | $2^{nd}$ | $33^{rd}$ | $1^{st}$ |
| matrix_mult_a | 66 | 65 | 78 | 74 | 72 | $30^{th}$ | $5^{th}$ | $1^{st}$ | $1^{st}$ | $5^{th}$ |
| matrix_mult_b | 63 | 62 | 76 | 73 | 76 | $22^{nd}$ | $93^{rd}$ | $4^{th}$ | $1^{st}$ | $4^{th}$ |
| Average | 65 | 66 | 77 | 74 | 76 | $32^{nd}$ | $27^{th}$ | $2^{nd}$ | $8^{th}$ | $3^{rd}$ |

TR: Trial Routing
GR: Global Routing

# #DRV Prediction Error vs. Time




- Y: gap between the 'best in 10' and the actually 1st-ranked placement with least #DRV
- X: inference time
- RouteNet achieves low inference time and high accuracy at the same time

# DRV Hotspot Detection

- Same decision threshold is used for all designs
- Slight different False Positive Rate (FPR), all under 1%
- RouteNet has the highest True Positive Rate (TPR)

| Circuit Name | FPR (%) | TPR (%) | | | | |
|---|---|---|---|---|---|---|
| | | TR | GR | LR | SVM | RouteNet |
| des_perf | 0.54 | 17 | 56 | 54 | 42 | 74 |
| edit_dist | 1.00 | 25 | 36 | 38 | 28 | 64 |
| fft | 0.30 | 21 | 45 | 54 | 31 | 71 |
| matrix_mult_a | 0.21 | 13 | 30 | 34 | 12 | 49 |
| matrix_mult_b | 0.24 | 13 | 37 | 41 | 20 | 53 |
| Average | 0.46 | 18 | 41 | 44 | 27 | 62 |

# Future Plan for Year 1

- Improving routability prediction by considering pin access
- Routability prediction for analog and mixed-signal IC designs
- Pre-routing timing prediction

# Students on Task 2810.021, 2810.022

- Zhiyao Xie, Duke University, expected graduation: 2021
- Rongjian Liang, TAMU, expected graduation: 2021
- Planned internship: Rongjian Liang, IBM, summer 2019

# Interactions with SRC Companies

- Regular web meetings with IBM
- Site visit to ARM
- Site visit to Mentor Graphics
- Web meeting with NXP

# Thank You!