

DEEP: <u>Developing Extremely Efficient</u> Runtime On-Chip Power Meters





In .fsdb/.vcd file format

Zhiyao Xie¹, Shiyu Li², Mingyuan Ma², Chen-Chia Chang², Jingyu Pan², Yiran Chen², Jiang Hu³

¹Hong Kong University of Science and Technology, ²Duke University, ³Texas A&M University



INTRODUCTION Temporal Claimed OPM Model Input Candidate V_M Baseline Methods (Candidate Count M) Area Overhead Resolution All RTL signals (178 K) B1. MICRO'21 [38] Per-cycle < 1% B2. MICRO'19 [20] All RTL signals (178 K) 100s cycles N/AB3. DATE'18 [25] Registers (67 K) > 1K cycles B4. DATE'18 [41] Module I/O signals (< 178K) 100s cycles 4 - 10%B5. ASPDAC'15 [39] Registers (67 K) Per-cycle 16% All bits of RTL signals (578 K) **DEEP** (this work) Per-cycle < 0.1% **Power** ν Λ cycle1 0 cycle2 | 0 | 0 | 1 cycle0 | 1 | 0 | 0 | 0 | 0 cycle1 0 1 1 0 0 cycle2 0 0 1 1 1 A design in RTL level. M RTL signals cycle0 cycle1 cycle2 Train the ML model: F(X) = y

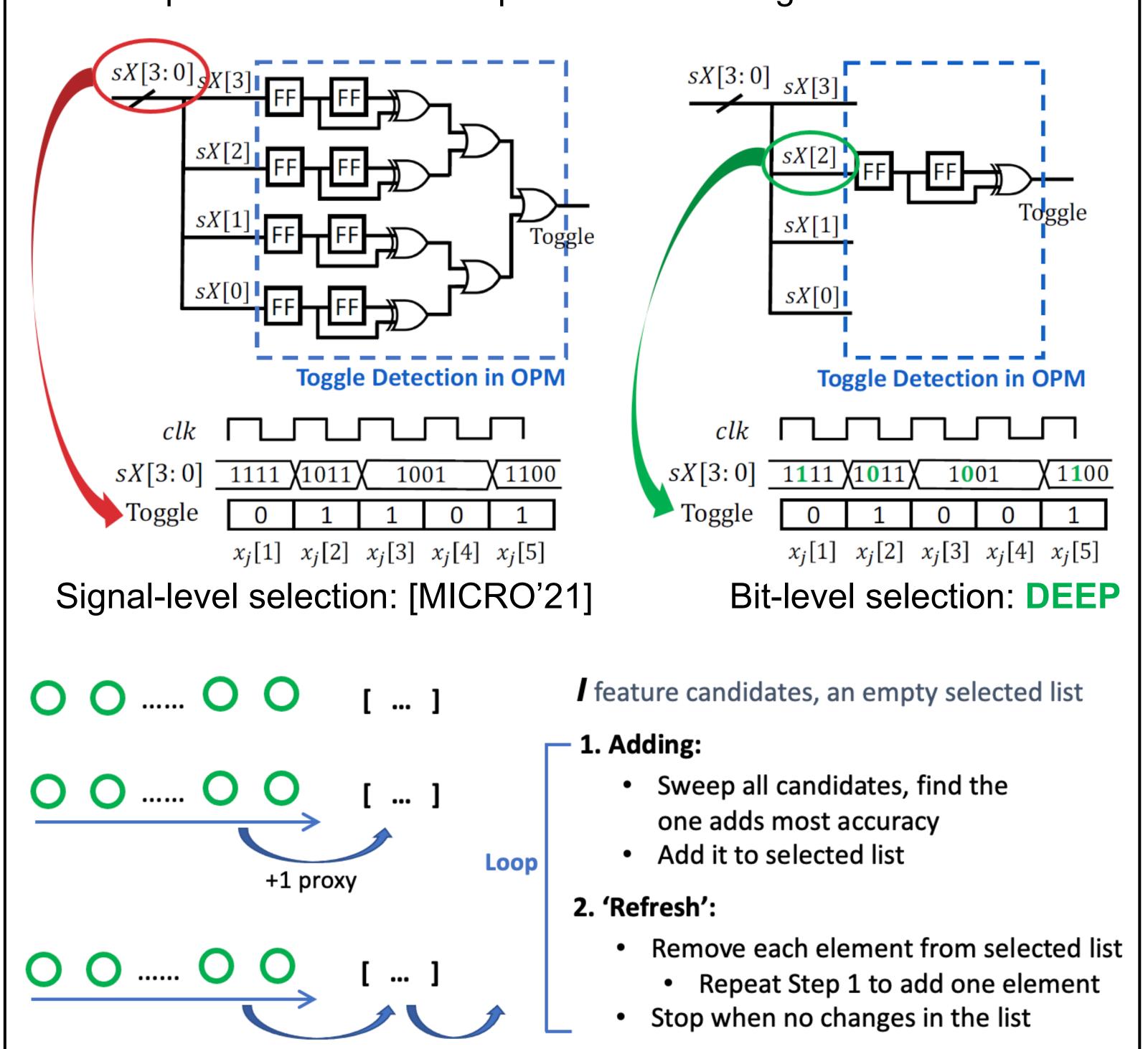
RTL of Arbitrary Training **Design Layout** RTL **Circuit Design** with OPM Simulation Testbench/ Synthesis Traces of Synthesis All Signals & Layout **DEEP** Integrate with Toggles of Power Layout All M Bits X Design RTL Simulation Select Q OPM **Power** [Implement] Power Model OPM Labels y RTL Proxies

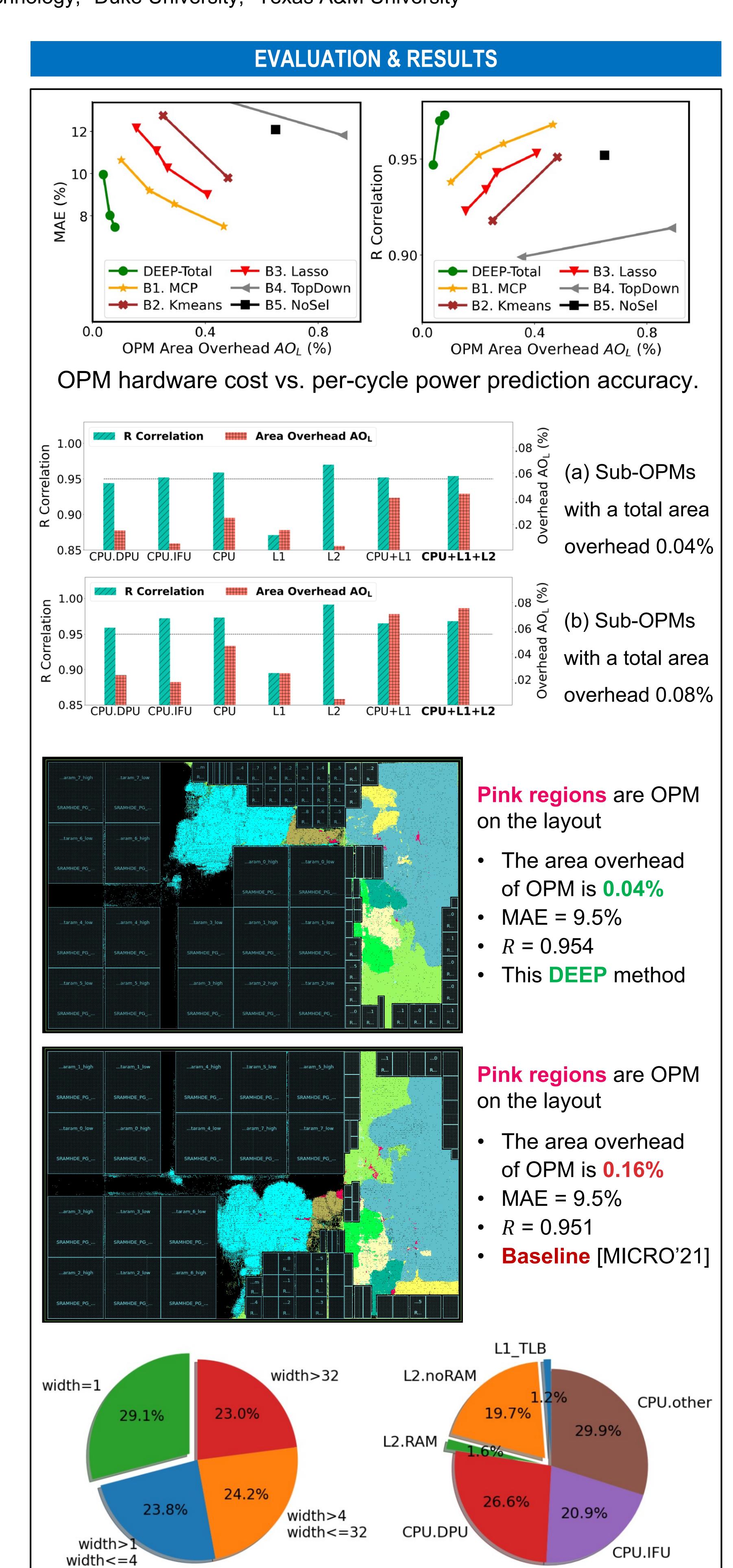
METHODOLOGY

- 1. Generate data with waveform of signals and power labels
- 2. Develop OPM by selecting minimum signals as input
- 3. Implement the OPM as part of circuit design

+1 proxy

-1 proxy





Analysis of 244 selected proxies.