

# ZHIYAO XIE

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## RESEARCH INTERESTS

- Electronic Design Automation, Machine Learning Algorithms, VLSI Design Flow

## ACADEMIC QUALIFICATIONS

- **Ph.D.** in Electrical and Computer Engineering, Duke University, 2022
- **B.Eng.** in Electronic and Communication Engineering, City University of Hong Kong, 2017

## PRESENT POSITION

- **Assistant Professor**, Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology (**HKUST**), June 2022 ~ Present

## SELECTED AWARDS & HONORS

- ACM Outstanding Dissertation Award in EDA (one awardee per year), 2023
- EDAA Outstanding Dissertation Award (one awardee per category), 2023
- ASP-DAC 2023 Best Paper Award, 2023
- ASP-DAC 2023 Best Paper Candidate, 2023
- ACM TODAES Distinguished Reviewer, 2022
- ACM SIGDA SRF Best Research Poster Award, 2022
- IEEE/ACM MICRO 2021 Best Paper Award (first author), 2021
- ECE Ph.D. Fellowship, Duke University, 2018
- Dean's List for all 8 semesters, CityU HK, 2013-2017
- Full Tuition Scholarship for 4 years, CityU HK, 2013-2017

## PEER-REVIEWED PUBLICATIONS

- [1] Afzal Ahmad, **Zhiyao Xie**, Wei Zhang, "PertNAS: Architectural Perturbations for Memory-Efficient Neural Architecture Search". *Design Automation Conference (DAC)*, 2023.
- [2] Jian PENG, Tingyuan Liang, **Zhiyao Xie**, Wei Zhang, "PROPHET: Predictive On-Chip Power Meter for Hardware DNN Accelerator". *Design Automation Conference (DAC)*, 2023.
- [3] **Zhiyao Xie**, "Efficient Runtime Power Modeling with On-Chip Power Meters (Invited)". *International Symposium on Physical Design (ISPD)*, 2023.
- [4] **Zhiyao Xie**, Tao Zhang, and Yifeng Peng, "Security and Reliability Challenges in Machine Learning for EDA: Latest Advances (Invited)". *International Symposium on Quality Electronic Design (ISQED)*, 2023.
- [5] Linfeng Du, Tingyuan Liang, Sharad Sinha, **Zhiyao Xie**, Wei Zhang. "FADO: Floorplan-Aware Directive Optimization for High-Level Synthesis Designs on Multi-Die FPGAs". *International Symposium on Field-Programmable Gate Arrays (FPGA)*, 2023.
- [6] Chen-Chia Chang, Jingyu Pan, **Zhiyao Xie**, Jiang Hu, Yiran Chen. "Rethink before Releasing your Model: ML Model Extraction Attack in EDA". *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2023. **(Best Paper Award)**
- [7] Chen-Chia Chang, Jingyu Pan, **Zhiyao Xie**, Yaguang Li, Yishuang Lin, Jiang Hu, Yiran Chen. "Fully Automated Machine Learning Model Development for Analog Placement Quality Prediction". *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2023. **(Best Paper Candidate)**
- [8] **Zhiyao Xie**, Jingyu Pan, Chen-Chia Chang, Jiang Hu, and Yiran Chen. "The Dark Side: Security and Reliability Concerns in Machine Learning for EDA". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022.

- [9] **Zhiyao Xie**, Rongjian Liang, Xiaoqing Xu, Jiang Hu, Chen-Chia Chang, Jingyu Pan, Yiran Chen, “Pre-Placement Net Length and Timing Estimation by Customized Graph Neural Network”. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022.
- [10] **Zhiyao Xie**, Shiyu Li, Mingyuan Ma, Chen-Chia Chang, Jingyu Pan, Yiran Chen, Jiang Hu. “DEEP: Developing Extremely Efficient Runtime On-Chip Power Meters”. *International Conference on Computer-Aided Design (ICCAD)*, 2022.
- [11] Jingyu Pan, Chen-Chia Chang, **Zhiyao Xie**, Jiang Hu and Yiran Chen. “Robustify ML-based Lithography Hotspot Detectors”. *International Conference on Computer-Aided Design (ICCAD)*, 2022.
- [12] Jingyu Pan, Chen-Chia Chang, **Zhiyao Xie**, Ang Li, Minxue Tang, Tunhou Zhang, Jiang Hu, and Yiran Chen. “Towards Collaborative Intelligence: Routability Estimation based on Decentralized Private Data”. *Design Automation Conference (DAC)*, 2022.
- [13] **Zhiyao Xie**, Xiaoqing Xu, Matt Walker, Joshua Knebel, Kumaraguru Palaniswamy, Nicolas Hebert, Jiang Hu, Huanrui Yang, Yiran Chen, Shidhartha Das, “APOLLO: An Automated Power Modeling Framework for Runtime Power Introspection in High-Volume Commercial Microprocessors”. *International Symposium on Microarchitecture (MICRO)*, 2021. **(Best Paper Award)**
- [14] Chen-Chia Chang, Jingyu Pan, Tunhou Zhang, **Zhiyao Xie**, Jiang Hu, Weiyi Qi, Chung-Wei Lin, Rongjian Liang, Elias Fallon, Yiran Chen, “Automatic Routability Predictor Development Using Neural Architecture Search”. *International Conference on Computer-Aided Design (ICCAD)*, 2021.
- [15] **Zhiyao Xie**, Rongjian Liang, Xiaoqing Xu, Jiang Hu, Yixiao Duan, Yiran Chen, “Net<sup>2</sup>: A Graph Attention Network Method Customized for Pre-Placement Net Length Estimation”. *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2021.
- [16] **Zhiyao Xie**, Hai Li, Xiaoqing Xu, Jiang Hu, Yiran Chen, “Fast IR Drop Estimation with Machine Learning (Invited)”. *International Conference on Computer-Aided Design (ICCAD)*, 2020.
- [17] **Zhiyao Xie**, Haoxing Ren, Brucek Khailany, Ye Sheng, Santosh A, Jiang Hu, Yiran Chen, “PowerNet: Transferable Dynamic IR Drop Estimation via Maximum Convolutional Neural Network”. *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2020.
- [18] **Zhiyao Xie**, Guan-Qi Fang, Yu-Hung Huang, Haoxing Ren, Yanqing Zhang, Brucek Khailany, Shao-Yun Fang, Jiang Hu, Yiran Chen, Erick Carvajal Barboza, “FIST: A Feature-Importance Sampling and Tree-Based Method for Automatic Design Flow Parameter Tuning”. *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2020.
- [19] Rongjian Liang, **Zhiyao Xie**, Jinwook Jung, Vishnavi Chauha, Yiran Chen, Jiang Hu, Hua Xiang, Gi-Joon Nam, “Routing-Free Crosstalk Prediction”. *International Conference on Computer-Aided Design (ICCAD)*, 2020.
- [20] Yu-Hung Huang, **Zhiyao Xie**, Guan-Qi Fang, Tao-Chun Yu, Haoxing Ren, Shao-Yun Fang, Yiran Chen, Jiang Hu, “Routability-Driven Macro Placement with Embedded CNN-Based Prediction Model”. *Design, Automation, and Test in Europe Conference (DATE)*, 2019.
- [21] **Zhiyao Xie**, Yu-Hung Huang, Guan-Qi Fang, Haoxing Ren, Shao-Yun Fang, Yiran Chen, Jiang Hu, “RouteNet: Routability Prediction for Mixed-Size Designs Using Convolutional Neural Network”. *International Conference on Computer-Aided Design (ICCAD)*, 2018.

## OTHER SELECTED PUBLICATIONS

- [1] **Zhiyao Xie**, Jingyu Pan, Chen-Chia Chang, Rongjian Liang, Erick Carvajal Barboza, and Yiran Chen, “Chapter 2: Deep Learning for Routability Prediction”. In Book: *Machine Learning Applications in Electronic Design Automation*. Springer, 2022.
- [2] Rongjian Liang, **Zhiyao Xie**, Erick Carvajal Barboza, and Jiang Hu, “Chapter 3: Net-Based Machine Learning-Aided Approaches for Timing and Crosstalk Estimation”. In Book: *Machine Learning Applications in Electronic Design Automation*. Springer, 2022.
- [3] **Zhiyao Xie**, “Intelligent Circuit Design and Implementation with Machine Learning”. *Ph.D. Dissertation of Duke University*, 2022. **(ACM Outstanding Dissertation Award in EDA) (EDAA Outstanding Dissertation Award)**

## SELECTED PRESENTATIONS

- [1] “Efficient Digital Design and Implementation with Machine Learning in EDA,” *AI Chip Center for Emerging Smart Systems (ACCESS)-CEDA Seminar Series*, 2022.
- [2] “DEEP: Developing Extremely Efficient Runtime On-Chip Power Meters,” *Conference Pre-Recorded Talk at ICCAD*, 2022.
- [3] “Exploring Design Solutions through AI-assisted Prediction and Parameter Tuning,” *ACCESS Technology Symposium on Frontiers of AI Accelerators*, 2022.
- [4] “Truly Intelligent Circuit Design and Implementation,” *Invited talk in Alibaba, AMD, Seminar at HKUST and CityU HK, HKUST ECE Department Talk*, 2022.
- [5] “The Best of EDA Research” (Co-presenter), *ACM/IEEE Design Automation WebiNar (DAWN)*. 2022.
- [6] “APOLLO: An Automated Power Modeling Framework for Runtime Power Introspection in High-Volume Commercial Microprocessors,” *Conference talk at MICRO, Invited Talk at Biren Technology, Oak Ridge National Lab, Livestream at AI Time, AI Tech Review*, 2021.
- [7] “Net2: A Graph Attention Network Method Customized for Pre-Placement Net Length Estimation,” *Conference talk at ASP-DAC*, 2021
- [8] “PowerNet: Transferable Dynamic IR Drop Estimation via Maximum Convolutional Neural Network,” *Conference talk at ASP-DAC, 1<sup>st</sup> MLCAD Workshop*, 2020.
- [9] “FIST: A Feature-Importance Sampling and Tree-Based Method for Automatic Design Flow Parameter Tuning,” *Conference talk at ASP-DAC, 1<sup>st</sup> MLCAD Workshop, SRC Techcon 2020*.
- [10] “A Collaborative Machine Learning Approach to Fast and High-Fidelity Design Prediction.” (Co-presenter) *Texas Analog Center of Excellence (TxACE) Symposium*, 2019.
- [11] “Deep Learning and GPU Acceleration for VLSI Physical Design” (Co-presenter), *Nvidia GPU Technology Conference (GTC)*, 2018.
- [12] “RouteNet: Routability Prediction for Mixed-Size Designs Using Convolutional Neural Network.” *Conference Talk at ICCAD*, 2018.

## PROFESSIONAL SERVICE

- Seminar Chair, IEEE CEDA Hong Kong, 2023
- Technical Program Committee Member of ICCAD 2023
- Technical Program Committee Member of ASP-DAC 2023
- Publicity Chair, IEEE CEDA Hong Kong, 2022
- Journal Reviewer of IEEE TCAD, ACM TODAES (Distinguished Reviewer), IEEE TCAS-I, IEEE ESL, IEEE Design & Test, IEEE CAL, ACM TECS, ACM JETC, Springer JCST, etc.

## PREVIOUS PROFESSIONAL EXPERIENCE

- Research Intern in Digital Circuit and System Group, **Arm**, June ~ Nov. 2020
- Research Intern in Digital Implementation Group, **Synopsys**, May ~ Aug. 2019
- Research Intern in ASIC & VLSI Research Group, **Nvidia**, Sept. ~ Dec. 2018
- Research Intern in Machine Learning for Layout Group, **Cadence**, June ~ Aug. 2018

## TEACHING EXPERIENCE

- Instructor of ELEC 2350. *Introduction of Computer Organization and Design*. HKUST, 2023.
- Instructor of ELEC 6950 A&B. *ECE Departmental Seminar*. HKUST, 2023.
- Instructor of ELEC 2910. *Academic and Professional Development*. HKUST, 2022-23.
- TA of ECE 586. *Vector Space Methods with Applications*. Duke University, 2021.
- EDA Admin & Supporter of ECE 532. *Analog Integrated Circuit Design*. Duke University, 2021.
- TA of ECE 350L. *Digital Systems*. Duke University, 2021.
- EDA Admin & Supporter of ECE 539. *CMOS VLSI Design Methodologies*. Duke University, 2020.